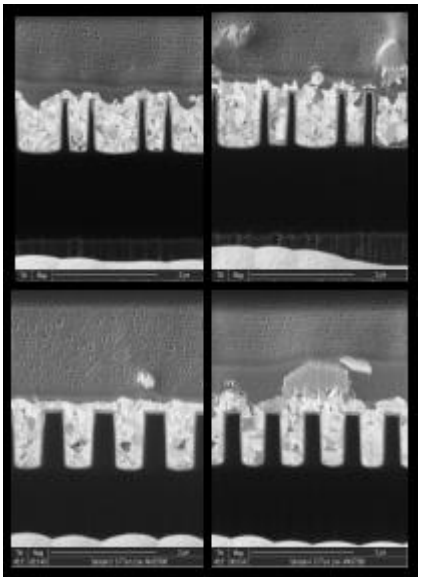
Copper Metallization for ULSI Applications using a FARADAYIC® Process

Objective:

This project demonstrated the feasibility of using the patented FARADAYIC® Process to deposit copper with minimal overplate, for ULSI features for semiconductor applications.

Summary:

The FARADAYIC® Process is used to develop a single step process for copper metallization and planarization for ULSI applications. The process is based on FARADAYIC® Leveling including a simple, robust $CuSO_4/H_2SO_4/PEG/Cl^-$ bath and yields: 1) void-free copper filling of trenches, and 2) conformal copper coating of trenches. Shown is metallization and planarization of a 0.25, 0.5 and 0.77 µm trench filled with copper. *NOTE: these examples illustrate the FARADAYIC® Leveling capability, any deviations in complete trench filling are due to a lack of initial copper deposition*. The FARADAYIC® Process gave 1) substantial reduction (~87%) in the waste associated with the current chemical-mechanical planarization process, 2) high plating rate, and 3) due to the absence of low concentration brighteners and levelers, a simple, easily controlled plating bath. Since the *Faradayic* approach consists of an infinite combination of forward, reverse and off-times, it is possible to "tune" the FARADAYIC® waveform for specific applications, provided one understands the nuances associated with the application. Future efforts will transition the FARADAYIC® Process technology from the bench to pilot scale: 1) demonstrate the FARADAYIC® process on 8-inch wafers, 2) develop a process library for feature sizes of interest to the VLSI/ULSI industry, *e.g.,* down to 90 nm, and lower, and 3) design a "proof of concept" plating tool incorporating Faraday's process module.



0.25 and 0.5 (top) and 0.77 (bottom) µm trenches

Background:

The patented FARADAYIC® Process is an electrochemical manufacturing technique that utilizes a controlled electric field to electrodeposit a material of interest. Since the FARADAYIC® Process is electrically mediated, it does not require small amounts of proprietary chemicals to facilitate the metal deposition as needed in conventional electrochemical processes (e.g. DC). The material deposition rate is determined by the applied electric field, which is user-defined and computer controlled. This provides the means for precise control of the length of the process, the total material deposited and the properties of the deposit.

The FARADAYIC® Process technology illustrated above is protected by a substantial patent portfolio including issued, allowed, and pending patent actions.

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