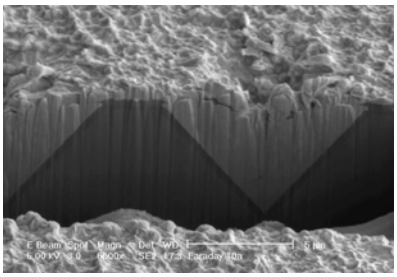
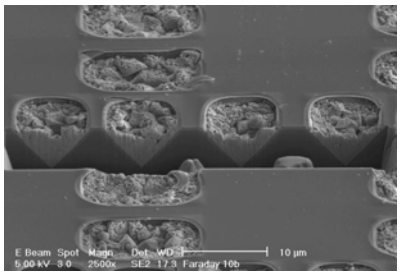
Copper Metallization for VLSI Applications using a FARADAYIC® Process

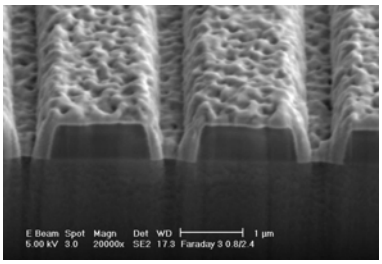
Objective:

This project demonstrated the feasibility of using the patented FARADAYIC® Process to deposit copper with minimal overplate, for VLSI features for semiconductor applications.

Summary:







The FARADAYIC® Process is used to develop a single step process for copper metallization and planarization for VLSI applications. The process is based on FARADAYIC® Leveling including a simple, robust $CuSO_4/H_2SO_4/PEG/Cl^-$ bath and yields: 1) void-free copper filling of trenches, and 2) conformal copper coating of trenches. Shown are a cross-section for filling a 5 µm trench, the capability to remove excess surface copper, as well as the copper seed layer, and conformal electrodeposition in a 0.8 µm trench. *NOTE: these examples illustrate the* FARADAYIC® *Leveling capability, any deviations in complete trench filling are due to a lack of initial copper deposition.*

The Faraday approach fully utilizes the potential of the FARADAYIC® Leveling process over a wide range of feature sizes (i.e., submicron-200 µm), to obtain both conformal electrodeposition and trench filling with minimal surface coverage. Since the FARADAYIC® Leveling approach consists of an infinite combination of forward, reverse and off-times, it is possible to "tune" the FARADAYIC® Leveling waveform for specific applications, provided one understands the nuances associated with the application. Specifically, the current distribution in the VLSI applications are governed by microprofile considerations under severely limited mass transport conditions.

Background:

The FARADAYIC® Process is an electrochemical manufacturing technique that utilizes a controlled electric field to electrodeposit a material of interest. Since the FARADAYIC® Process is electrically mediated, it does not require small amounts of proprietary chemicals to facilitate the metal deposition as needed in conventional electrochemical processes (e.g. DC). The material deposition rate is determined by the applied electric field, which is user-defined and computer controlled. This provides the means for precise control of the length of the process, the total material deposited and the properties of the deposit.

The FARADAYIC® Process technology illustrated above is protected by a substantial patent portfolio including issued, allowed, and pending patent actions.

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