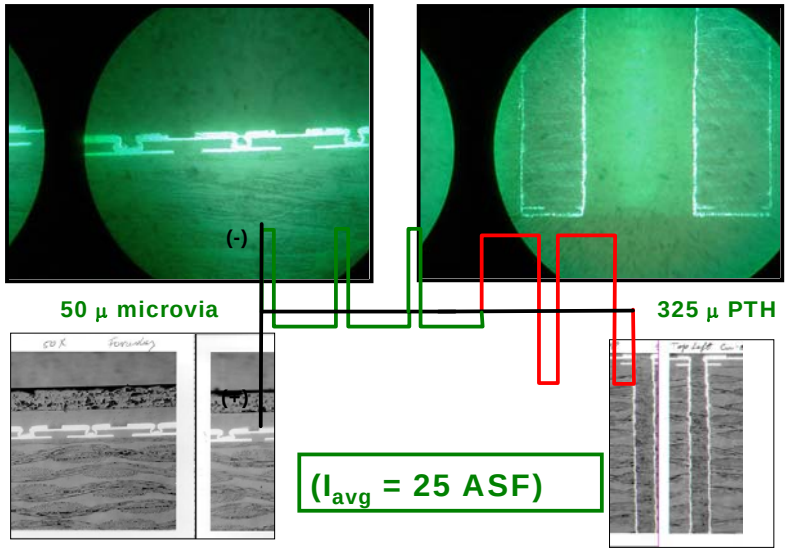
Sequential Plating of Multiple Features Using the FARADAYIC® Process

Objective:

This project demonstrated the ability to deposit copper into multiple feature sizes on a printed circuit board in one process step using the sequential patented FARADAYIC® Process.

Summary:

A FARADAYIC® Process successfully deposited copper into z-axis interconnects for HDI substrates. Instead of conventionally used "brighteners", "levelers" and/or "suppressors", the FARADAYIC® Process uses an electrically mediated waveform to control the current distribution, and therefore the distribution of copper in microvias and plated through-holes (PTHs). Since the FARADAYIC® approach controls the copper plating process by electric field mediation rather than chemical mediation, different features on the same substrate may be plated from the same plating bath by sequentially tuning the *Faradayic* Process parameters. The ability to sequentially copper plate microvias and PTHs was demonstrated on a one third scale PWB panel at 30 mA/cm^2 without masking. This work and related work has demonstrated the effectiveness of FARADAYIC® Process to copper plate features ranging from 0.25 μm to 325 μm.



Background:

The patented FARADAYIC® Process is an electrochemical manufacturing technique that utilizes a controlled electric field to electrodeposit a material of interest. Since the FARADAYIC® Process is electrically mediated, it does not require small amounts of proprietary chemicals to facilitate the metal deposition as needed in conventional electrochemical processes (e.g. DC). The material deposition rate is determined by the applied electric field, which is user-defined and computer controlled. This provides the means for precise control of the length of the process, the total material deposited and the properties of the deposit.

The FARADAYIC® Process technology illustrated above is protected by a substantial patent portfolio including issued, allowed, and pending patent actions.

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