

FARADAYIC® Wafer Processing Tool

Objective:

This wafer processing tool was developed to incorporate and demonstrate the capabilities of using the patented FARADAYIC® Process to deposit or etch copper for semiconductor applications.

Summary:

Faraday has established an in-house, three-station wafer processing tool. This pilot-scale facility replicates the functionality of state-of-the-art commercial production lines and incorporates advance cell design concepts including virtual anodes and a moving cathode. The three stations are currently dedicated to non-contact polishing of low-k wafer substrates, electrodeposition of copper onto wafer substrates, and electrodeposition of lead-free tin solders onto wafer substrates.

Background:

Faraday's wafer processing tool has been financially supported by the National Science Foundation and the Faraday Technology Marketing Group, an intellectual property asset management company.

Operation of this pilot-scale facility is in conjunction with Dynatronix, a market leader for advanced electroplating rectification equipment, and Prof. Alan West of Columbia University, a recognized expert in the field.

The facility's mission is to advance the state-of-the-art for processing features on semiconductor wafers, including advances in electroplating and non-contact polishing.

The FARADAYIC® Process technology illustrated above is protected by a substantial patent portfolio including issued, allowed, and pending patent actions.

